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MAY 8 2003 C133 Docket No.: GR 00 P 1679

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By: *[Signature]*

Date: April 28, 2003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Dieter Kantz et al.
Applic. No. : 09/826,594
Filed : April 5, 2001
Title : Test Configuration for the Functional Testing of a Semiconductor Chip
Examiner : Ernest F. Karlsen - Art Unit: 2829

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. 1.97(C)(1)

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

United States Patent No. 5,130,645 (Levy), dated July 14, 1992;

Korean Office Action dated March 12, 2003.

In accordance with 37 C.F.R. 1.97(e) the undersigned herewith states that each item of information contained in the information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

In accordance with 37 C.F.R. 1.97 (c) (1), consideration of this Information Disclosure Statement is requested.

Respectfully submitted,



For Applicants

Mark P. Weichselbaum
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Date: April 28, 2003

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))		Attorney Docket No.: GR 00 P 1679	Applic. No. 09/826,594
		Applicant Dieter Kantz et al.	
		Filing Date April 5, 2001	Group Art Unit 2829

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A	5,130,645	07/14/92	Levy			
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
	J						
	K						
	L						
	M						
	N						

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	O	
	P	

EXAMINER DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609;
 Draw line through citation if not in conformance and not considered. Include copy of this form with
 next communication to applicant.

Notice to File a Response

Applicant's Name: Infineon Technologies AG

Attorney's Name: Sang-sun NAM

Patent Appln. No.: 10-2001-0017980

Title of Invention: Test arrangement for testing function of a semiconductor chip

We hereby inform you of the following reason(s) for rejection pursuant to Article 63 of the Korean Patent Act. The applicant, if needed, may file an argument and an amendment no later than **May 12, 2003**.

R E A S O N

Since the invention in claim 1 of the present application could have been easily conceived from the document indicated below prior to the filing of the present application by a person having ordinary knowledge in the art to which the present invention pertains, the present invention cannot be patented according to Article 29(2) of the Korean Patent Act.

DETAILED GROUNDS

Claim 1 of the present invention relates to a test configuration having a self-test unit, comprising a power source connected to the semiconductor chip. However, USP 5,130,645 (July 14, 1992) discloses a built-in self-test structure, comprising a power supply circuit connected to a semiconductor chip. Thus, the invention of claim 1 of the present invention could have been easily conceived from the cited invention.

[Attachment]

1. A copy of USP 5,130,645 (July 14, 1992)

Date: March 12, 2003

Examiner: J. W. OH

Examination Bureau IV

Korean Intellectual Property Office